



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

John W. ANDREWS et al.

Serial No.: 09/883,981

Group Art Unit: 2813

Filed: June 20, 2001

Examiner: David S. Blum

For: LOW COST SHALLOW TRENCH ISOLATION USING NON-CONFORMAL
DIELECTRIC MATERIAL

Honorable Commissioner of Patents
Washington, D.C. 20231

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TECHNOLOGY CENTER 2800

AMENDMENT UNDER 37 C.F.R. §1.111

Sir:

In response to the Office Action dated April 2, 2002, please amend the above-identified application as follows:

IN THE CLAIMS:

Please amend the claims to read as follows:

SUB E1 8. (Twice Amended) A semiconductor substrate comprising:
D1 at least one trench comprising seamless filler material having an upper surface which is unpolished and co-planar with a upper surface of said substrate.

SUB E2 15. (Twice Amended) A semiconductor substrate having a planarized trench region
D2 formed according to a method comprising:
forming a pad on a surface of said substrate;
forming at least one trench in said substrate;
applying a seamless filler material by high density plasma method in said at least one trench and on said pad;
selectively removing said filler material on said pad so as to separate said filler material in said at least one trench and said filler material on said surface by an exposed area of said pad,
removing said filler material on said pad,